CLAIMS

What is claimed is:

1. A CMOS or NMOS device having one or more n-channel FETs disposed on a substrate, the device being resistant to total dose radiation failures, the device further comprising a negative voltage source, for applying a steady negative back bias to said substrate to mitigate leakage currents in said device, thereby mitigating total dose radiation effects.

2. The device of claim 1, wherein said back bias is less than the breakdown voltage of drain-substrate and source-substrate junctions, and greater than zero.

3. The device of claim 1, wherein said back bias is between about −5 V and about −0.1 V.

4. The device of claim 1, wherein said back bias is between about −3 V and about −1 V.

5. The device of claim 1, wherein said CMOS device is engineered to have a threshold voltage within a selected operating range while said steady negative voltage is applied.

6. The device of claim 5, wherein said operating range is between 0 V and 0.8 V.

7. A method for operating a CMOS or NMOS device to resist total dose radiation effects, said CMOS device having one or more n-channel FETs disposed on a substrate, comprising the steps:

selecting a maximum ionizing radiation dose for operation of said CMOS or NMOS device; and

determining and applying a negative back bias to said substrate of said CMOS or NMOS device, wherein said negative back bias is sufficient to essentially eliminate leakage currents in a field region of said CMOS or NMOS device, thereby providing hardness against said maximum ionizing radiation dose.

8. The method of claim 7, wherein said negative back bias is a steady negative back bias.

9. The method of claim 7, wherein said negative back bias is a variable negative back bias.

10. The method of claim 7, wherein said CMOS or NMOS device is engineered to have a threshold voltage within a selected operating range while said steady negative voltage is applied.

11. The method of claim 10, wherein said operating range is between 0 V and 0.8 V.